

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1, 2, 4-5, 16-18, 27-30 and 35-38 are pending in this application and were rejected under 35 U.S.C. §102(b) as being anticipated by Kuwabara (JP 06-069509).

The Applicant respectfully requests withdrawal of the finality of this rejection. The Applicant made no changes to the claims in the prior response, yet the claims are now rejected on a new basis using a different reference than the rejections in the prior Office Action. The new rejection is necessitated due to the Applicant overcoming the previous prior art rejection, and not due to amendments of the claims by the Applicant. Therefore, it is respectfully requested that the finality of the outstanding Office Action be withdrawn.

As pointed out in the previous response, the invention of claim 1 relates to, in an electrode contact section incorporated into a semiconductor substrate and having an impurity layer and a contact layer, the location of the peak of the impurity concentration in each of the impurity and contact layers. In the contact section of claim 1, the peak of the impurity concentration of the impurity layer is at a point more than 0.2 and not more than 1.0 μm from the surface of the semiconductor substrate, and the peak of the impurity concentration of the contact layer is at a point not more than 0.2 μm from the surface of the semiconductor substrate. Such a section has superior characteristics, as described before.

Turning to the 35 U.S.C. §102 rejection, according to the Office Action, Kuwabara discloses (i) an anode region 11 having a thickness of 10 μm or less, and (ii) a p⁺ anode region 21 formed thereon and having a thickness of 0.1 to 1.0 μm . The Office Action finds this disclosure in Kuwabara to teach the contact section of claim 1 or the device of claim 16. However, the contact section of claim 1 and the device of claim 16 are not disclosed in Kuwabara.

Kuwabara may refer to the depth of an impurity layer but does not disclose anything about the peak point of the impurity concentration of that impurity layer. First, it must be understood that the peak point of the impurity concentration of an impurity layer differs from the depth of the impurity layer. The peak point of the impurity concentration is a point where the impurity concentration is highest, and can be definitely determined. On the other hand, the “depth” of an impurity concentration is vague, and it is hard to determine which point in the concentration is referred to in connection with the depth. Unless the definition of “depth” is clearly determined, it is not possible to determine the peak point of the impurity concentration.

Kuwabara does not disclose the definition of the “depth” for the anode layers and therefore does not disclose anything about the peak point of the impurity concentration. Kuwabara cannot therefore disclose the contact section having the impurity layer and contact layer of claim 1, or the device having the impurity region and contact region of claim 16.

Further, according to the translation provided by the USPTO, region 21 is polycrystalline silicon formed by “vapor growth” on substrate 1 or, more precisely, on region 11 (see paragraph [0016]). Region 21 is not formed in region 11. In claim 1 the contact layer is formed in the impurity layer, and the impurity layer is formed in one surface of the substrate. In claim 16 the contact region is formed in the impurity region and the impurity region is formed in a surface of the semiconductor substrate. The translation provided by the USPTO does not disclose or suggest the section of claim 1 or the device of claim 16.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

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